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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/549,678	PELEG, ZOHAR	
	Examiner	Art Unit	
	Kenan Cehic	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. In addition to Replacement Sheets containing the corrected drawing figure(s), applicant is required to submit a marked-up copy of each Replacement Sheet including annotations indicating the changes made to the previous version. The marked-up copy must be clearly labeled as "Annotated Sheets" and must be presented in the amendment or remarks section that explains the change(s) to the drawings. See 37 CFR 1.121(d)(1). Failure to timely submit the proposed drawing and marked-up copy will result in the abandonment of the application.

Claim Objections

3. Claim 5, 8, 9, 16-18 are objected to because of the following informalities:

As regarding claim 5, for "CEP" in line 1 and 3, the full written meaning needs to be provided.

As regarding claim 8, "a segment base-address" in line 1 seems to refer back to the same limitation in claim 1 line 6. If that correct it is suggested to applicant to change this limitation to --said segment base-address-- .

As regarding claim 8, "a byte offset" in line 8 seems to refer back to the same limitation in claim 8 line 7. If that correct it is suggested to applicant to change this limitation to -- said byte offset-- .

As regarding claim 9, "a plurality of hierarchically arranged queues" in line 1 seems to refer back to the same limitation in claim 6 line 2. If that correct it is suggested to applicant to change this limitation to --said plurality of hierarchically arranged queues -- .

As regarding claim 16, "a channel hierarchy" in line 1 and 2 seems to refer back to the same limitation in claim 15 line 3. If that correct it is suggested to applicant to change this limitation to --said channel hierarchy -- . Similar problems exist in claim 17 line 1.

As regarding claim 18, "a CH-ID number" in line 1 seems to refer back to the same limitation in claim 17 line 2. If that correct it is suggested to applicant to change this limitation to –said CH-ID number -- .

Appropriate action is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
a.

4. Claim 1 is recites the limitation "said respective packet sequential number" in line There is insufficient antecedent basis for this limitation in the claim.

It is not know which of the "for each packet a packet sequential number" of claim 1 line 5 the applicant is referring to.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claim 10, 11 rejected under 35 U.S.C. 102(e) as being anticipated by Isukapalli et al (US 7,126,957).

For claim 10, Isukapalli et al discloses a hierarchically partitioned (see Figure 3B, 304-0, 304-3, 304-7; note channel order) jitter buffer memory (see Figure 3b, Jitter Buffer)

comprising: a. a plurality of hierarchically arranged (see Figure 3B, 304-0, 304-3, 304-7; note channel order) queues (see Figure 3B, 304-0, 304-3, 304-7 and column 4 lines 25-30 "write to synchrounous ...read data...from jitter buffer ....to ...local buffer") correlated with a channel hierarchy (see Figure 3B, 304-0, 304-3, 304-7; note channel order); and b. a mechanism (see Figure 2, 206) for addressing (see Figure 2, 206, "generate jitter buffer address", "write jitter buffer data to locat buffer according to channel id") said hierarchically arranged queues (see Figure 3B, 304-0, 304-3, 304-7 and column 4 lines 25-30 "write to synchrounous ...read data...from jitter buffer ....to ...local buffer").

For claim 11, Isukapalli et al discloses said hierarchically arranged queues (see Figure 3B, 304-0, 304-3, 304-7 and column 4 lines 25-30 "write to synchrounous ...read data...from jitter buffer ....to ...local buffer") are

further divided into segments (see Figure 3B, 304-3, t0, t1, t2) each said segment (see Figure 3B, 304-3, t0, t1, t2) designed to hold one packet (see column 8 lines 11-14 "channel...payload may be written to the CH3 t2 location in region 304-3").

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim 1, 3, 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isukapalli et al (US 7,126,957) in view of Sherman (US 6,831,912).

For claim 1, Isukapalli discloses a method for partitioning allocation (see Figure 3B, 304-0, 304-3, 304-7) and management (see Figure 2, 200 and Figure 6a-b, 600) of jitter buffer memory (see Figure 3b, Jitter buffer) for

TDM (see column 6 lines 24-26 "TDM") circuit emulation applications (see Figure 1, "Asynchronous System" and "Synchronous System" and column 6 lines 39-43 "between asynchronous formats and synchronous formats") comprising the steps of:

a. obtaining (see column 7 lines 1-3 "getting...number of channels" and Figure 6b, "get channel value") a channel hierarchy (see Figure 6b "get channel Value (CH)" and Figure 3b, 304-0, 304-3, 304-7; note ascending channel number order) for a plurality of packet carrying (see column 4 lines 15-18 "packet") channels (see Figure 6b, "for each channel" and column 4 lines 15-18 "channels" and column 7 lines 1-7 "different channels....different voice channels") having different channel rates (see column 11 23-35 "different time-out....different rate than other");

b. obtaining (see Figure 6a, 602, "read...sequence #") for each packet (see Figure 6a, "upon packet reception") a respective packet sequential number (see Figure 6a "602 "read...sequence # "); and

c. generating a segment base-address (see column 8 lines 5-10 "if a channel is active, a jitter buffer address is calculated".A jitter buffer address may be calculated according to a jitter buffer size, channel value and time indication...particular jitter buffer location for a channel (eg. 304-0" and see Figure 2, 304-0; column 9 lines 16-21 "begin at a base address") in the jitter buffer memory (see Figure 3b, Jitter buffer) using said channel hierarchy (see column 4 lines 20-24" channel value" and see column 8 lines 5-10 "channel value") and said respective packet sequential number (see column 8 lines 6-8 "time indication" and column 14 lines 56-60 "pointer to a jitter buffer entry...a sequence number for the packet saved");

whereby said partitioning allocation (see Figure 3B, 304-0, 304-3, 304-7) and management (see Figure 2, 200 and Figure 6a-b, 600) of the jitter buffer memory (see Figure 3b, Jitter buffer) is

correlated (see Figure 3B, 304-0, 304-3, 304-7 and Figure 6a, 600) with said generated segment base-address (see column 8 lines 5-10 "if a channel is active, a jitter buffer address is calculated".A jitter buffer address may be calculated according to a jitter buffer size, channel value and time indication...particular jitter buffer location for a channel (eg. 304-0" and see Figure 2, 304-0; column 9 lines 16-21 "begin at a base address") such that each said channel see Figure 6b, "for each channel" and column 4 lines 15-18 "channels" and column 7 lines 1-7 "different channels.....different voice channels") is allocated a space (see Figure 3B, 304-0, 304-3, 304-7) , in a buffer memory (see Figure 3b, "Jitter Buffer") of a given size (see Figure 3B, 304-0, 304-3, 304-7), and whereby out-of-order packets (see column are automatically reordered (see column 9 lines 57-63 "may be written to jitter buffer location according to a time indication value in a packet, thus accounting for ...order for a given channel") by the jitter buffer (see column 9 lines 57-63 "jitter buffer").

For claim 3, Isukapalli et al discloses said step of obtaining a channel hierarchy (see Figure 6b "get channel Value (CH)") further includes obtaining a channel identification (CH-ID) number (see Figure 6b "get channel Value (CH)").

For claim 6, Isukapalli et al discloses wherein said generating a segment base-address (see column 8 lines 5-10 "if a channel is active, a jitter buffer address is calculated".A jitter buffer address may be calculated according to a jitter buffer size, channel value and time indication...particular jitter buffer location for a channel (eg. 304-0" and see Figure 2, 304-0; column 9 lines 16-21 "begin at a base address") in the jitter buffer memory (see Figure 3b, Jitter buffer) includes dividing (see Figure 3B, 304-0, 304-3, 304-7) said jitter

buffer memory (see Figure 3b, Jitter buffer) into a plurality of hierarchically (see Figure 3B, 304-0, 304-3, 304-7; note channel order) arranged queues (see Figure 3B, 304-0, 304-3, 304-7 and column 4 lines 25-30 "write to synchrounous ...read data...from jitter buffer ....to ...local buffer") and allocating each said queue (see Figure 3B, 304-0, 304-3, 304-7 and column 4 lines 25-30 "write to synchrounous ...read data...from jitter buffer ....to ...local buffer") to one said channel (see Figure 3B, 304-0, 304-3, 304-7, CH 0, CH 3, CH 7) , so that the queue hierarchy (see Figure 3B, 304-0, 304-3, 304-7) follows said channel hierarchy (see Figure 3B, 304-0, 304-3, 304-7, CH 0, CH 3, CH 7; notice ascending order)

Isukapalli et al is silent about:

As regarding claim 1, said space being proportional to a respective said channel rate.

Sherman from the same or similar field of endeavor discloses a communications system with the following features:

As regarding claim 1, Sherman discloses said space being proportional (see column 2 lines 46-50 "size of ...buffer is a function...data rate associated with the channel") to a respective said channel rate (see column 2 lines 46-50 "size of ...buffer is a function...data rate associated with the channel").

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Isukapalli et al by using the features, as taught by Sherman, in order to provide to provide enough memory storage to adequately accommodate the speed of a communications link.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isukapalli et al (US 7,126,957) in view of Sherman (US 6,831,912) , as applied to claim 1 above, further in view of Nigam et al (US 2005/0135436).

For claim 2, the claimed invention is described as in paragraph 6.

Isukapalli further discloses, as regarding claim 2, a step of obtaining a channel hierarchy (see column 7 lines 1-3 "getting...number of channels" and Figure 6b, "get channel value") includes obtaining a channel hierarchy (see Figure 6b "get channel Value (CH)") for at least two of channels (See Figure 3b, CH 0, CH 3) of said plurality (see Figure 6b, "for each channel" and column 4 lines 15-18 "channels" and column 7 lines 1-7 "different channels....different voice channels").

Isukapalli and Sherman are silent about:

As regarding claim 2, that channels include packets of different size.

Nigam from the same or similar field of endeavor discloses a TDM network with the following features:

As regarding claim 2, Nigam discloses that channels (See Figure 2, lines connecting network elements and section 0022 lines 3-9 "lines....optical line transmitting SONET OC-N signals") include packets of different size (see section 0047 lines 1-18 "STS-1....STS-3....STS-12,STS-48, STS-192"....OC-12....OC-3,...OC1, OC6 or OC12").

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Isukapalli et al and Sherman by using the features, as taught by Nigam, in order to incorporate any size and location of concatenated SONET frames (see section 0015 lines 1-14).

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isukapalli et al (US 7,126,957) in view of Sherman (US 6,831,912) , as applied to claim 1 above, further in view of Gavrilovich (US 5,729,826).

For claim 4, the claimed invention is described as in paragraph 6.

Isukapalli further discloses, for claim 4, said obtaining of a CH-ID number (see Figure 6b "get channel Value (CH)") includes obtaining a CH-ID number(see Figure 6b "get channel Value (CH)").

For claim 4, Isukapalli and Sherman are silent about:

As regarding claim 4, a CH-ID number of 9 bits.

Gavrilovich from the same or similar field of endeavor discloses:

As regarding claim 4, a CH-ID number of 9 bits (see column 8 lines 34-36 "channel...9 identification bits").

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Isukapalli et al and Sherman by using the features, as taught by Gavrilovich, in order to provide 512 unique identifications numbes (see column 8 lines 36-37).

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isukapalli et al (US 7,126,957), Sherman (US 6,831,912) and Gavrilovich (US 5,729,826), as applied to claim 1 above, further in view of Ben-David (US 6,273,622) and Andrew G Malis et al. , "SONET/SDH Circuit Emulation over Packet (CEP)" (July 2002)

For claim 5, the claimed invention is described in paragraph 8.

For claim 5, Isukapalli, Sherman, and Garvrilovich are silent about:

As regarding claim 5, wherein each said packet includes a CEP header, and wherein said step of obtaining a packet sequential number includes obtaining a 14 bit sequential number from said CEP header.

Ben-David from the same or similar field of endeavor discloses a data communication protocol with the following features:

each said packet includes a CEP header (see Figure 9, "CEP HEADER"), and wherein said step of obtaining (see column 10 lines 5-12 "CEP process implement..monitors difference between the Sequential Message Number ....") a packet sequential number (see Figure 9, "Sequential Message number")

Andrew G Malis et al. from the same or similar field of endeavor disclose the CEP header:

14 bit sequential number (see Section "4.2 CEP Header", Figure 2 – Basic CEP Header Format, "Sequence Number [0:13]) from said CEP header (see Section "4.2 CEP Header", Figure 2 – Basic CEP Header Format, "Sequence Number [0:13]").

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Isukapalli et al, Sherman, and Gavrilovich by using the features, as taught by Ben-David and Andrew G. Malis, in order to provide detection of and recovery from packet loss and extreme network congestion (see Ben-David column 2 lines 7-10); and in order to conform with the IETF CEP header requirements.

10. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isukapalli et al (US 7,126,957), Sherman (US 6,831,912), as applied to claim 6 above, further in view of Dreibelbis et al (US 5,875,470).

For claim 7, the claimed invention is described in paragraph 6.

Isukapalli further discloses for claim 7, a step of generating a segment base-address (see column 8 lines 5-10 "if a channel is active, a jitter buffer address is calculated".A jitter buffer address may be calculated according to a jitter buffer size, channel value and time indication...particular jitter buffer location for a channel (eg. 304-0" and see Figure 2, 304-0; column 9 lines 16-21 "begin at a base address") and the jitter buffer (see Figure 3b, Jitter buffer)

Isukapalli and Sherman are silent about:

As regarding claim 7, determining an address size based on said jitter buffer memory size.

Dreibelbis from the same or similar field of endeavor discloses a memory component with the following features:

Dreibelbis discloses, for claim 7, determining (see column 5 lines 6-8 "receives and handles....compatible") an address size (see column 5 lines 6-8 "address size") based on memory size (see column 5 lines 6-8 "memory size").

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Isukapalli et al and Sherman by using the features, as taught by Dreibelbis, in order to provide an address variable whose size can accommodate the available memory space.

11. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isukapalli et al (US 7,126,957), Sherman (US 6,831,912), as applied to claim 6 above, further in view of Spencer (US 2004/0243739).

For claim 9, the claimed invention is described as in paragraph 6.

Isukapalli further discloses, for claim 9, wherein said dividing said jitter buffer memory (see Figure 3B, 304-0, 304-3, 304-7) into a plurality of hierarchically arranged queues (see Figure 3B, 304-0, 304-3, 304-7; note channel order) includes partitioning said jitter buffer memory (see Figure 3B, 304-0, 304-3, 304-7) into said queues (see Figure 3B, 304-0, 304-3, 304-7) .

Isukapalli and Sherman are silent about:

As regarding claim 9, using powers of 2 division factors.

Spencer from the same or similar field of endeavor discloses a memory access with the following features :

Spencer discloses using powers of 2 division factors (see section 0014 lines 14-18 "size...queue...multiple of 16-bytes....4KB in size")

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Isukapalli et al and Sherman by using the features, as taught by Spencer, in order to provide an memory space that is conforms to widely used standards of using multiple of 2 to border memory space.

12. Claim 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isukapalli et al (US 7,126,957) in view of Kasper (US 2006/0212633).

For claim 12, Isukapalli discloses the claimed invention as described in paragraph 5.

Isukapalli further disclose, for claim 12, segments (see Figure 3B, 304-3, t0, t1, t2) is characterized carried by a respective said channel (see column 8 lines 11-14 "channel...payload may be written to the CH3 t2 location in region 304-3").

Isukapalli further disclose, for claim 13, number of said segments (see Figure 3B, 304-3, t0, t1, t2) in bytes (see column 14 line 32 "number of octets received" and column 5 lines 62-67 "jitter buffer...1 data byte...4 bytes..8 bytes") is an integer power of 2 (column 5 lines 62-67 "jitter buffer...1 data byte...4 bytes..8 bytes")

Isukapalli further disclose, for claim 14, segment size (see column 8 lines 11-14 "channel...payload may be written to the CH3 t2 location in region 304-3"; segments adjusts to any payload size) is that can hold said maximum packet size (see column 8 lines 11-14 "channel...payload may be written to the CH3 t2 location in region 304-3"; segments adjusts to any payload size).

Isukapalli is silent about:

As regarding claim 12, by a size in bytes correlated with a maximum packet size .

As regarding claim 13, is an integer power of 2.

As regarding claim 14, the minimum integer power of 2

Kasper from the same or similar field endeavor discloses a method for routing data over a network with the following features:

As regarding claim 12, by a size in bytes (see section 0171 lines 15-20 "256 bytes...2000 or 5000 bytes") correlated with a maximum packet size (see section 0171 lines 15-20 "size is selected based upon the maximum supported frame size")

As regarding claim 13, Kasper discloses is an integer power of 2 (see section 0171 lines 15-20 "256 bytes").

As regarding claim 14, the minimum integer power of 2 As regarding claim 13, Kasper discloses is an integer power of 2 (see section 0171 lines 15-20 "256 bytes").

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Isukapalli et al by using the features, as taught by Kasper, in order to provide adequate memory size for the maximum data units that a network device can receive and to provide a hybrid option between a store and forward architecture and a cut through architecture (see section 0015).

13. Claim 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isukapalli et al (US 7,126,957) in view of Nigam et al. (US 2005/0135436)

For claim 15, Isukapalli discloses method for partitioning allocation (see Figure 3B, 304-0, 304-3, 304-7) and management (see Figure 2, 200 and Figure 6a-b, 600) of jitter buffer memory (see Figure 3b, Jitter buffer) for TDM (see column 6 lines 24-26 "TDM") circuit emulation applications (see Figure 1, "Asynchronous System" and "Synchronous System") comprising the steps of:

a. obtaining (see column 7 lines 1-3 "getting...number of channels" and Figure 6b, "get channel value") a channel hierarchy (see Figure 6b "get channel Value (CH)" and Figure 3b, 304-0, 304-3, 304-7; note ascending channel number order) for a plurality of packet (see column 4 lines 15-18 "packet")carrying channels see Figure 6b, "for each channel" and column 4 lines 15-18 "channels" and column 7 lines 1-7 "different channels....different voice channels")

having different channel rates (see column 11 23-35 "different time-out....different rate than other");

b. dividing (see Figure 3B, 304-0, 304-3, 304-7) the jitter buffer memory (see Figure 3b, Jitter buffer) into a plurality of hierarchically arranged

queues (see Figure 3B, 304-0, 304-3, 304-7; note channel order) queues (see Figure 3B, 304-0, 304-3, 304-7 and column 4 lines 25-30 "write to synchrounous ...read data...from jitter buffer ....to ...local buffer"); and

c. allocating (see Figure 3B, 304-0, 304-3, 304-7; note channels) each said hierarchically arranged queue (see Figure 3B, 304-0, 304-3, 304-7; note channel order) queues (see Figure 3B, 304-0, 304-3, 304-7 and column 4 lines 25-30 "write to synchrounous ...read data...from jitter buffer ....to ...local buffer") to a respective said channel (see Figure 3B, 304-0, 304-3, 304-7; note channels) so that said queue hierarchy follows said channel hierarchy (see Figure 3B, 304-0, 304-3, 304-7; note channel order) queues (see Figure 3B, 304-0, 304-3, 304-7 and column 4 lines 25-30 "write to synchrounous ...read data...from jitter buffer ....to ...local buffer"; note ascending order following channel numbers) ;

whereby the jitter buffer memory (see Figure 3b, Jitter buffer) can be advantageously optimized for TDM (see column 6 lines 24-26 "TDM") emulation (see Figure 1, "Asynchronous System" and "Synchronous System")

For claim 17, Isukapalli et al discloses said step of obtaining a channel hierarchy (see Figure 6b "get channel Value (CH)") further includes obtaining a channel identification (CH-ID) number (see Figure 6b "get channel Value (CH)").

Isukapalli is silent about:

As regarding claim 15, by a hierarchical partitioning can be assigned that follows the SONET/SDH hierarchy.

As regarding claim 16, obtaining a channel hierarchy includes obtaining a channel hierarchy for at least two of channels of said plurality that include packets of different size.

Nigam from the same field of endeavor discloses a TDM circuit emulation with the following features:

As regarding claim 15, by a hierarchical partitioning (see Figure 23a, 664, 664-a and see section 0125 lines 1-4 "descriptor ring...typically ring buffers, that are allocated for each of the channels") can be assigned that follows the SONET/SDH hierarchy (see section 0125 lines 1-4 "descriptor ring...typically ring buffers, that are allocated for each of the channels" and section 0078 lines 7-8 "channels are formed using ...STS-1, STS-3(c), STS-12...STS-48").

As regarding claim 16, obtaining a channel hierarchy includes obtaining a channel hierarchy (see Figure 23a, 664, 664-a and see section 0125 lines 1-4 "descriptor

ring...typically ring buffers, that are allocated for each of the channels") for at least two of channels of said plurality (section 0078 lines 7-8 "channels are formed using ...STS-1, STS-3(c), STS-12...STS-48") that include packets

of different size (section 0078 lines 7-8 "channels are formed using ...STS-1, STS-3(c), STS-12...STS-48").

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Isukapalli et al by using the features, as taught by Nigam et al., in order to provide a SONET-over-packet emulation to reduce cost and increase connectivity by being able to communicate synchronous signals over packet networks (see section 0006).

14. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isukapalli et al (US 7,126,957) in view of Nigam et al. (US 2005/0135436) , as applied to claim 17 above, further in view of Gavrilovich (US 5,729,826).

For claim 18, the claimed invention is described as in paragraph 13.

Isukapalli further discloses, for claim 4, said obtaining of a CH-ID number (see Figure 6b "get channel Value (CH)") includes obtaining a CH-ID number(see Figure 6b "get channel Value (CH)").

For claim 18, Isukapalli and Sherman are silent about:

As regarding claim 18, a CH-ID number of 9 bits.

Gavrilovich from the same or similar field of endeavor discloses:

As regarding claim 18, a CH-ID number of 9 bits (see column 8 lines 34-36 "channel...9 identification bits").

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Isukapalli et al and Sherman by using the features, as taught by Gavrilovich, in order to provide 512 unique identifications numbes (see column 8 lines 36-37).

15. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Isukapalli et al (US 7,126,957) in view of Nigam et al. (US 2005/0135436) , as applied to claim 15 above, further in view of Mann et al (US 2005/0220111).

For claim 19, the claimed invention is described as in paragraph 13.

For claim 19, Isukapalli further discloses said dividing (see Figure 3B, 304-0, 304-3, 304-7) the jitter buffer memory (see Figure 3b, Jitter buffer) into a plurality of hierarchjcally arranged (see Figure 3B, 304-0, 304-3, 304-7; note channel order) queues (see Figure 3B, 304-0, 304-3, 304-7 and column 4 lines 25-30 "write to synchrounous ...read data...from jitter buffer ....to ...local buffer") includes partitioning (see Figure 3B, 304-0, 304-3, 304-7) said jitter buffer memory (see Figure 3b, Jitter buffer) into said queues (see Figure 3B, 304-0, 304-3, 304-7 and column 4 lines 25-30 "write to synchrounous ...read data...from jitter buffer ....to ...local buffer").

Isukapalli and Nigam are silent about:

As regarding claim 19, by using powers of 2 division factors.

Mann et al from the same or similar field of endeavor disclose a processing optimization with the following features:

As regarding claim 19, by using powers of 2 division factors (see section 0029 lines 13-17 "size of the packet queue....6000 bytes")

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system of Isukapalli et al and Nigam by using the features, as taught by Mann et al, in order to optimize ingress processing via traffic classification and grouping (see section 0018).

Allowable Subject Matter

16. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Additionally, the rejection under 112 2nd set forth in this action need to be overcome.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenan Cehic whose telephone number is (571) 270-3120. The examiner can normally be reached on Monday through Friday 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang Yao can be reached on (571) 272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KC

KWANG BIN YAO
SUPERVISORY PATENT EXAMINER